DR. ADITYA KUMAR SINGH PUNDIR

Professor, Department of Electronics & Communication Engineering (NBA Accredited)
Arya College of Engineering & I.T., Jaipur , Rajasthan India (NAAC 'A', Autonomous)
Affiliation: Rajasthan Technical University, Kota, Rajasthan India

Chief Investigator, C2S Program, MEITY, GOVT. Of India
Organizing Chair, ICRTCIS Conference Series (https://www.icrtcis.in/)
Coordinator: Mentor Incubation & Research/IPR (R & D CELL AND IPR CELL)
LMISTE | MACM | LMCSI |LM Vijnana Bharati (VIBHA)|

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PROFESSIONAL SUMMARY

Experience (15 +)

- 15+ years of combined academic and industry experience (Suzlon Energy Ltd.; Z-Drive Software Pvt. Ltd.)

Technical Expertise

- Reconfigurable Hardware–VLSI, Embedded System Design, Edge AI Computing, BIST & Fault Tolerance

Academic Roles

- Professor (ECE); Mentor Incubation & Research/IPR Coordinator; IQAC member; IIC Steering Member,
- IPR CELL and R & D Cell @ Arya College of Engineering and I.T.
- M.Tech. Coordinator (JNU Jaipur), NAAC SOET coordinator (JNU Jaipur)

Publications

- 50+ peer-reviewed publications [12-SCI|SCIE|ESCI/26-Scopus], 10 books (Springer, IOP Science, SCRS, IET-IEEE)

IPR Leadership

- 78+ IPR applications filed;
  - 5 Patent Granted
  - 5 Design Application Granted
  - 2 Software Copyrights, 1 Literary Work Copyright

Governance

- Research Coordinator, IPR activity coordinator
- IQAC Member; Convener NAAC Criteria 3; Convener NBA Criteria 5,
- Past: M.Tech. Coordinator, Exam coordination, BOS member, SOET-NAAC Coordinator, NIRF Innovation contributor, 50+ FDPs/STTPs/workshops, Organizing Secretary and Convener - IAET Conference Series, RTVES Seminar Series

PROFESSIONAL MEMBERSHIPS

LMISTE: Life Member, Indian Society for Technical Education

MIEEE: Member, Institute of Electrical and Electronics Engineers (Past)

LMVIBHA: Life Member Vijnana Bharati (VIBHA)

MACM: Member, Association for Computing Machinery

LMCSI: Life Member, Computer Society of India

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ACADEMIC QUALIFICATIONS (HONORS DEGREE)

Doctor of Philosophy (Ph.D.)

- Specialization in Fault-Tolerant Reconfigurable Hardware Design using BIST Technique on SRAM
- VLSI FPGA based Reconfigurable Hardware and Memory Design and Testing, AI repair with Embedded System Firmware Development
- Focus on VLSI & Embedded Systems (Edge-AI Computing)

Master of Technology (M.Tech.)

- Specialization in VLSI Design
- Advanced coursework in semiconductor design, layout optimization, and verification techniques

Bachelor of Engineering (B.E.)

- Specialization in Electronics & Communication Engineering

12^{th} (PCM) : 78.92% | 10^{th}: 85.17%

CURRENT POSITION & INSTITUTIONAL ROLES

Primary Role

- Professor, Department of Electronics & Communication Engineering, Arya College of Engineering & I.T., Jaipur

Innovation Leadership| Institutional Contributions

- IPR CELL and R & D Cell @ Arya College of Engineering and I.T.
- Mentor Incubation & Research/IPR Activities Coordinator, Contributor, NIRF Innovation ranking parameters and documentation

Quality Assurance Roles

- IQAC Member; Convener NAAC Criteria 3; Convener NBA Criteria 5

Innovation Governance

- Steering Member, Institute Innovation Council (IIC)

Academic Governance

- Member, Board of Studies (BOS)

Registered Ph.D. Supervisor

- Rajasthan Technical University, Kota
- Office Order: RTU/Dean/ (R)/F (45)/ 2024 /1053-1062, Dated: 16/03/2024
- Currently supervising 1 Ph.D. candidates on **Deep fake Detection with Multimode Signals with Deep-Learning and AI**
- One Ph.D. Student completed Ph.D. on **IOT based Memory Repair** at Amity University, Rajasthan

LEADERSHIP EXPERIENCE

M.Tech Coordinator (JNU Jaipur)

- M.Tech. in Embedded System
- M.Tech. in Communication and Signal Processing

NAAC Coordination

- IQAC Member; Convener NAAC Criteria 3;
- Convener NBA Criteria 5,
- NAAC Coordinator: SoET, Jaipur National University

Research and Innovation Leadership

- IPR CELL and R & D Cell @ ACEIT: Overseeing research initiatives and innovation activities

Accreditation & Quality

- Led NAAC/NBA documentation, audits, and outcome-based education processes as Criteria Convener

Academic Administration

- Planning and development
- Research mentoring for students and faculty

Academic Events and International Conferences

Organizing **Six Months Advance Certification Program on Silicon to Systems: Advanced VLSI, Mixed-Signal & FPGA Design** supported by **Chipin Centre, C2S Program MeitY Govt. of India**

5+ DST-CIPAM, DPIIT IPR Activities

Organized 50+ FDP/STTP/workshops/conferences with support from TEQIP-III, AICTE, DST, CSIR-CEERI, and DRDO

Role: Organizing Chair, ICRTCIS (Springer) conference series; facilitated knowledge exchange platforms

- **International Conference on Recent Trends in Communication and Intelligent Systems** (ICRTCIS): ICRTCIS 2026, ICRTCIS 2025, ICRTCIS 2024, ICRTCIS 2022, ICRTCIS 2021, ICRTCIS 2020, ICRTCIS 2019
- **International Conference on Artificial Intelligence and Machine Learning** (ICAIML)
- **Innovative Advancement in Engineering and Technology** (IAET)
- **Recent Trends in VLSI and Embedded Systems** (RTVES)
- Publishers: **Springer Nature, IET-IEEE, SCRS , IGI Global, IOP Science, AIP**

RESEARCH FUNDING & PROJECTS

Project	Funding Agency	Amount (INR)	Status
Project/ Grant Running			
C2S Programme	MEITY, Govt of India	C2S, SMDP (Tools above 10 CRS)	Running
Embedded System development and Design **20 Kits from Renesas Quickconnect beginners kit-2.0**	Renesas Electronics Corporation	20000	Received, Development and Design: TBA
Project/ Grant Completed			
3rd International Conference on Recent Trends in Communication and Intelligent Systems, ICRTCIS 2021.	AICTE under Grant for Organizing Conference (GOC), AQIS Application ID: 1-9288904253, F.No. 67-39/IDC/GOC/POLICY-1/2020-21	2,94,200 utilized 50000 for Online Conference	Completed
"Adaptive Bio-Impedance Based Monitoring System for Medical and Industrial Applications" TEQIP III Collaborative Research Scheme, , Grant No. 1-5737385093, from 18th June 2019 to 30 June 2021	TEQIP III Collaborative Research Scheme, NPIU	411000	Completed
Springer International Conference on Recent Trends in Communication & Intelligent Systems on June 08-09, 2019	TEQIP III RTU (ATU)	Upto 500000 utilized 115000	Completed
National level Seminar on Recent Trends in VLSI & Embedded Systems (RTVES-2014)	DRDO	50000	Completed

RESEARCH EXPERTISE AND TECHNOLOGY FOCUS

Core Domains

- Reconfigurable Hardware–VLSI
- Embedded Systems Design
- Edge-AI Computing
- Optimization

Technical Strengths

- AI- Memory Repair Fault Tolerance Architectures
- BIST/DFT Methodologies
- FPGA/ASIC Design Flows
- Device Modeling
- Computer Architectures
- Microcontrollers and Embedded Systems
- Real-time Systems

Current Industry Trends Leveraged

- Intel Edge AI Engineer
- NPTEL Certification
- AI-for-EDA Tools
- System Development and IP Conversion

Lab/Tools Capabilities

- Chief Investigator: C2S Program, MEITY Govt. of India: Access to C2S/SMDP EDA Suite
- Handling tools and Licenses of above 10 CRs
- Implemented and Setup two labs for Semiconductor Fabless Design and FPGA Prototyping
- IoT/Edge Development Stacks

PUBLICATIONS & ACADEMIC CONTRIBUTIONS

40+ Research Publications

- Peer-reviewed papers in reputed journals and conferences
- SCI & Scopus-indexed journals
- International conferences proceedings

10+ Books Published

- Edited/authored with leading publishers
- Springer International Publishing
- IOP Science, SCRS Publishers

10+ Conference Organization

- Chair of international conferences
- ICRTCIS 2019 (TEQIP III RTU-ATU supported)
- ICRTCIS 2021 (AICTE GOC grant: ₹2,94,200)

50+ Academic Events

- Organized with funding from national bodies
- FDPs, STTPs, workshops with DST, CSIR-CEERI, DRDO
- Curriculum development, OBE implementation
- Research and Innovation mentoring

INTELLECTUAL PROPERTY RIGHTS (IPR) PORTFOLIO | INNOVATION & INCUBATION ACTIVITIES

78+ Total IPR Applications

- Processed, drafted, and filed for the College
- Comprehensive IP portfolio development
- 10 grants secured across categories

14+ Patent Applications

- Technical innovations and novel solutions
- 5 Patents granted
- 10 Patents in publication stage

8+ Designs & Copyrights

- Visual innovations and creative works
- Designs: 6 (5 granted, 1 in FER stage)
- Copyrights: 3 (all granted)

100% Campus Impact

- Building institutional IP culture
- End-to-end IP pipeline: ideation → drafting → filing → FER Response → Hearing and Defending → Grant
- IP awareness programs and mentorship
- 15+ events for IPR and Incubation Promotions and Management`
- Innovation Ambassador

KEY ACHIEVEMENTS & IMPACT

Accreditation Leadership

- Led quality assurance initiatives with significant outcomes
- Plan and Contributed to ECE NBA accreditation success, also as a Criteria 5 Convener
- Key role in NAAC 'A' grade achievement, Criteria 3, IPR Cell and R & D Cell

Chief Investigator C2S Program

- Chief Investigator: C2S Program, MEITY Govt. of India: Access to C2S/SMDP EDA Suite
- Handling tools of above 10 CRs
- Implemented and Setup two labs for Semiconductor Fabless Design and FPGA Prototyping
- IoT/Edge Development Stacks

Handling Research and Innovation Ecosystem: IPR Cell and R & D Cell

Built robust research ecosystem

- IPR applications filed across domains
- End-to-end IP pipeline: ideation → drafting → filing → FER Response → Hearing and Defending → Grant
- Enhanced lab infrastructure and grant success

50+ Academic Events

- Organized high-impact knowledge exchanges
- FDP/STTP/Workshops with national support
- Established ICRTCIS conference brand

Ph.D. and Research Scholar Development

- Mentoring next-gen researchers
- PhD scholars under supervision
- Project-to-patent and publication pathways

VISION FOR [DEAN – INNOVATION & RESEARCH| VICE CHANCELLOR]

Strategic Objectives

- Elevate Innovation & Research Cell profile and impact
- Accelerate IP commercialization pathways
- Expand sponsored research portfolio
- Establish strategic industry MoUs for collaboration

First 90 Days Plan

- Conduct comprehensive research capability audit
- Refresh IP policy and commercialization framework
- Develop EDA-lab utilization and optimization plan
- Launch internal seed-grant program for promising research
- Organize FDPs on VLSI/Edge AI technologies
- Establish internal review panels for research proposals

12-Month Targets

- 15+ quality IPR filings with commercialization potential
- 2+ sponsored research projects from government/industry
- 3+ industry MoUs with technology partners
- Increase C2S Program awareness and participation with Tape-out outcome
- Host a national-level conference on emerging tech trends

Key Performance Indicators

- IPR metrics: filings, grants, and commercialization attempts
- Funded projects: count, funding amount, and research output
- Publication impact: SCI/Scopus papers, citations, h-index
- NIRF Innovation score improvement year-over-year
- Student startup count and funding secured
- Industry engagement frequency and outcomes

THANK YOU

Feel free to contact:

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